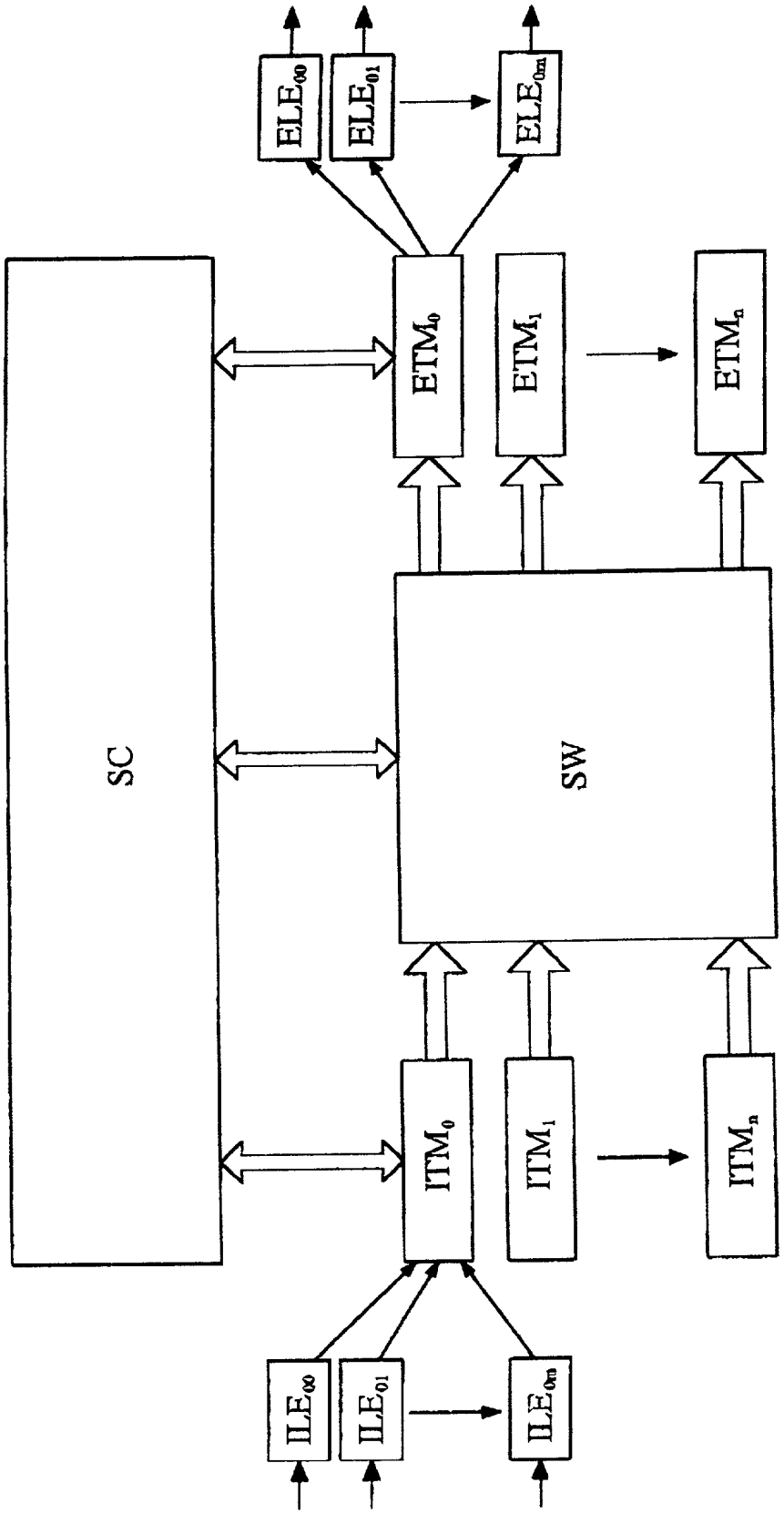

ELE00
ELE01
ELE0m
ETM0
ETM1
ETMn
SC
SW
ITM0
ITM1
ITMn
ILE00
ILE01
ILE0m

*Fig. 1*

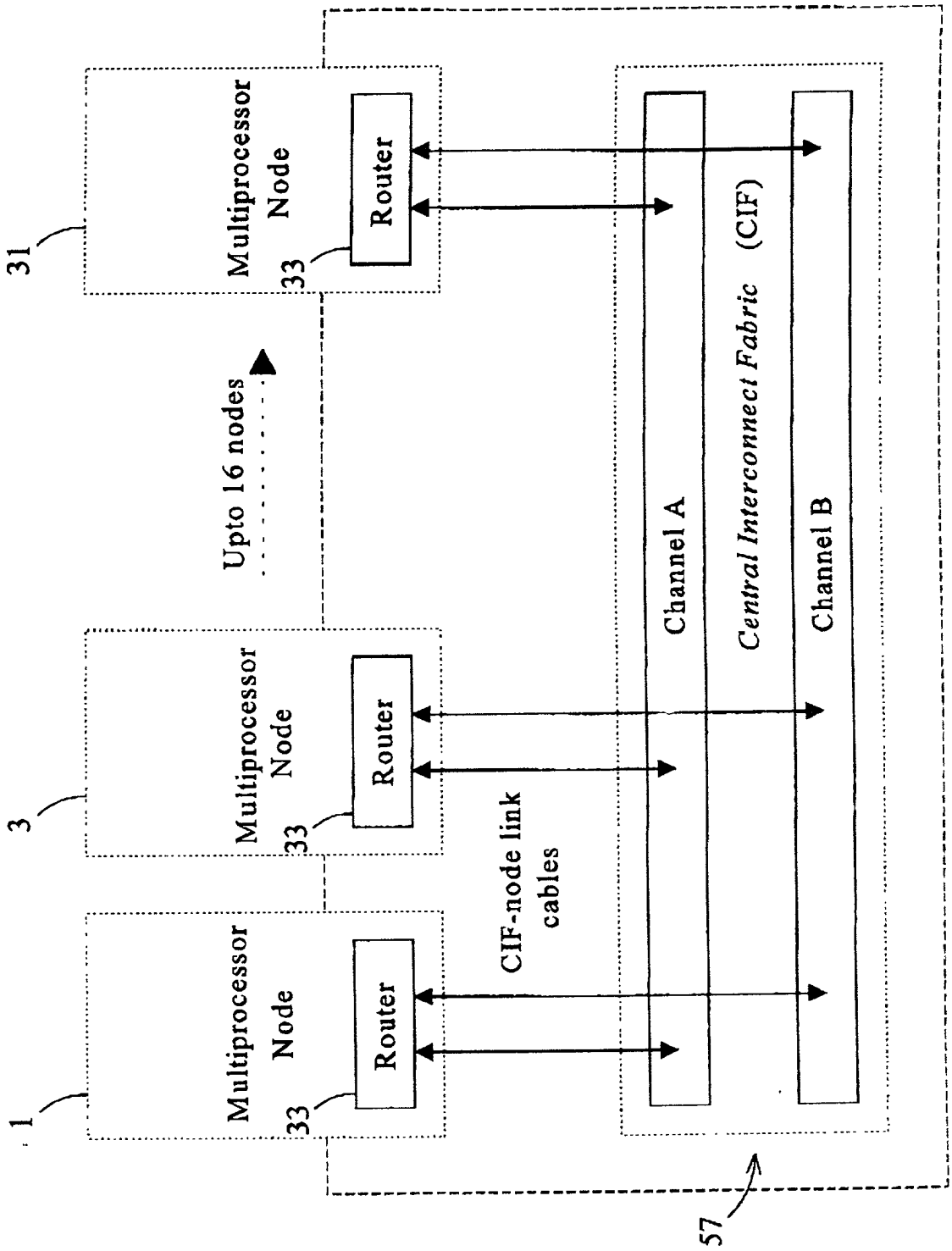

1
Multiprocessor Node
33
Router
3
Multiprocessor Node
33
Router
Upto 16 nodes
31
Multiprocessor Node
33
Router
CIF-node link cables
Channel A
Central Interconnect Fabric (CIF)
Channel B
57

*Fig. 2*

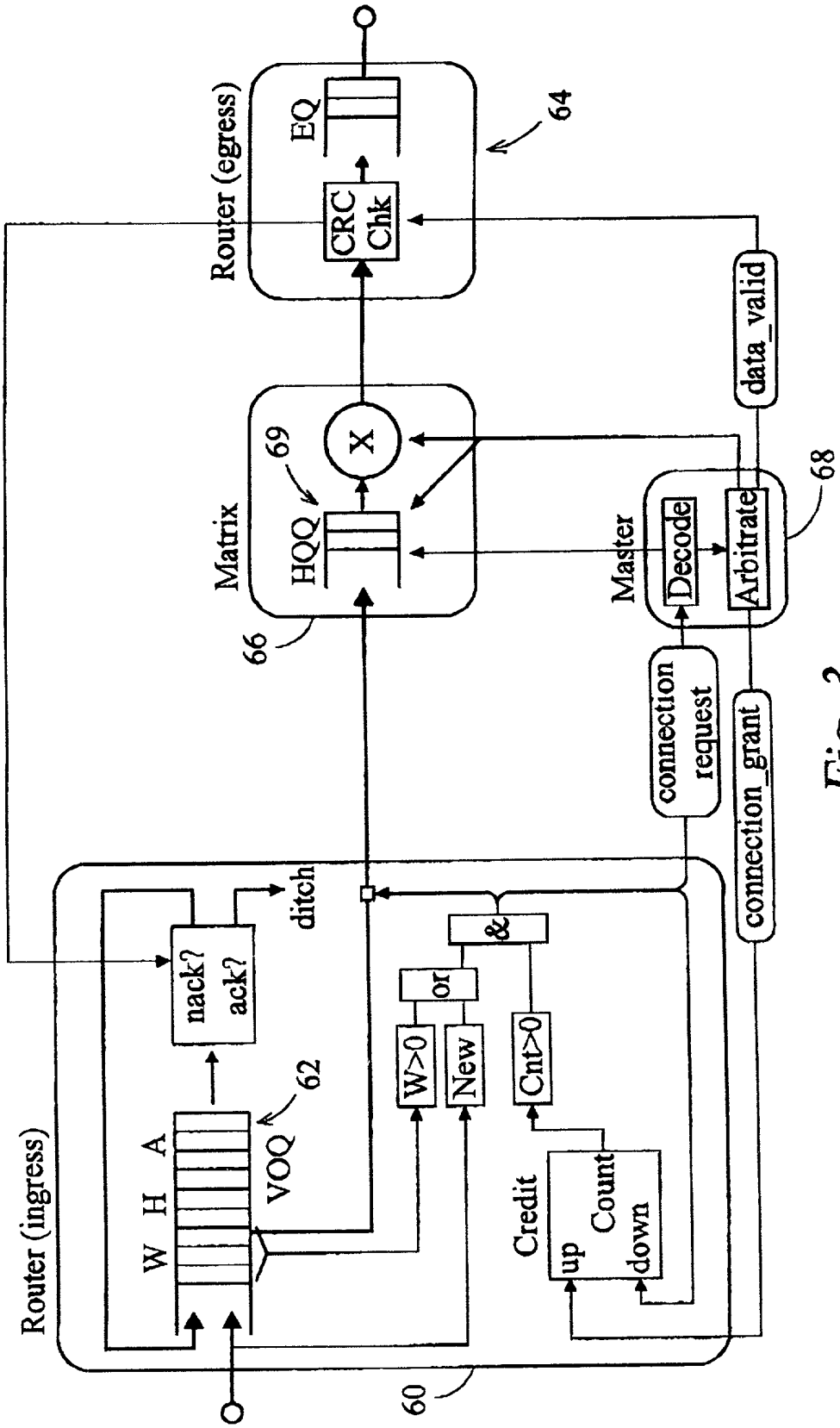
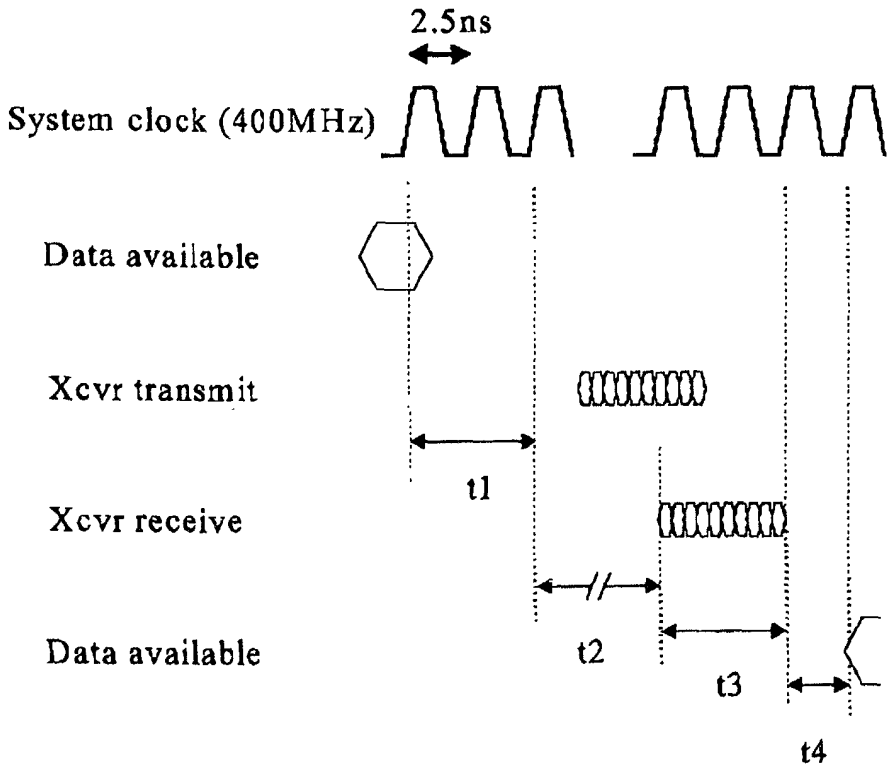

Router (egress)
EQ
CRC Chk
64
Matrix
69
HQQ
X
66
Master
Decode
Arbitrate
68
data_valid
connection request
connection_grant
Router (ingress)
W H A
VOQ
62
nack? ack?
ditch
W>0
New
or
&
Cnt>0
Credit
up
Count
down
60

*Fig. 3*




t1 = Router end data delay (2 cycles)

t2 = propagation delay + alignment delay (1 cycle min.)

t3 = byte period (2 cycles)

t4 = Matrix/Master end data delay (1 cycle)



*Fig. 4*

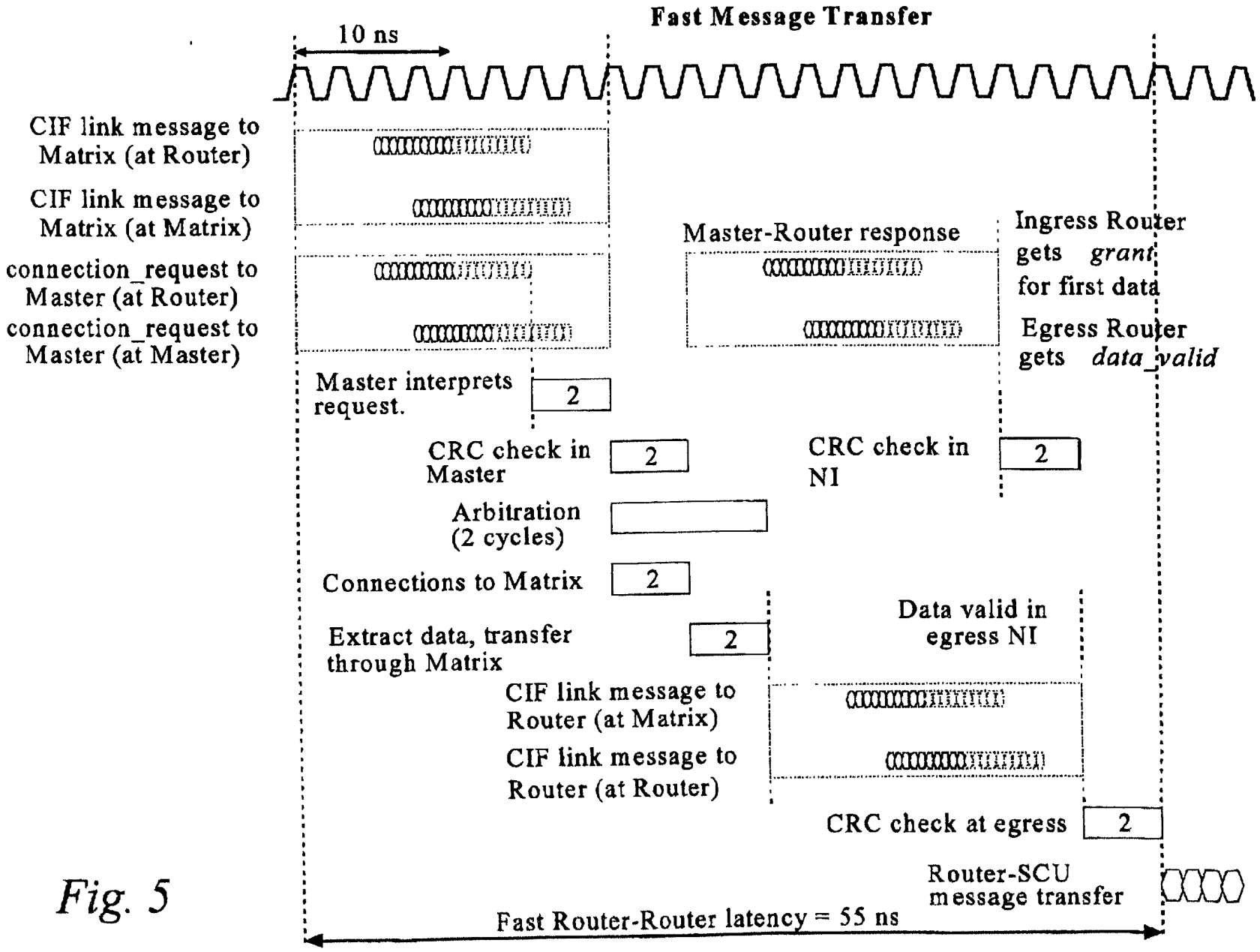

Fast Message Transfer
10 ns
CIF link message to Matrix (at Router)
CIF link message to Matrix (at Matrix)
connection_request to Master (at Router)
connection_request to Master (at Master)
Master-Router response
Ingress Router gets grant for first data
Egress Router gets data_valid
Master interprets request.
2
CRC check in Master
2
CRC check in NI
2
Arbitration (2 cycles)
Connections to Matrix
2
Extract data, transfer through Matrix
2
Data valid in egress NI
CIF link message to Router (at Matrix)
CIF link message to Router (at Router)
CRC check at egress
2
Router-SCU message transfer
Fast Router-Router latency = 55 ns

*Fig. 5*

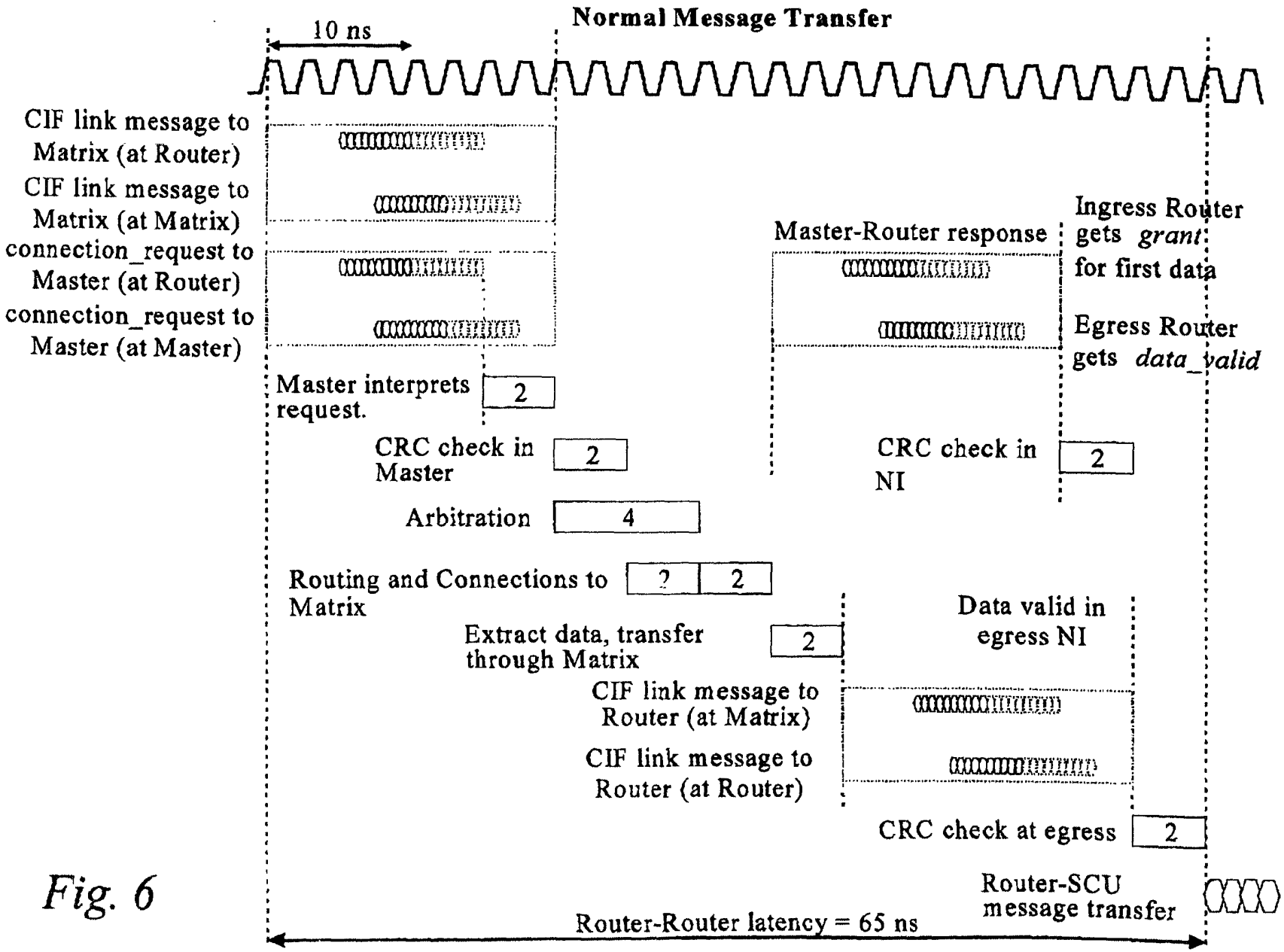

Normal Message Transfer
10 ns
CIF link message to Matrix (at Router)
CIF link message to Matrix (at Matrix)
connection_request to Master (at Router)
connection_request to Master (at Master)
Master interprets request.
2
CRC check in Master
2
Arbitration
4
Routing and Connections to Matrix
?
2
Extract data, transfer through Matrix
2
CIF link message to Router (at Matrix)
CIF link message to Router (at Router)
Master-Router response
Ingress Router gets grant for first data
Egress Router gets data_valid
CRC check in NI
2
Data valid in egress NI
CRC check at egress
2
Router-SCU message transfer
Router-Router latency = 65 ns

*Fig. 6*

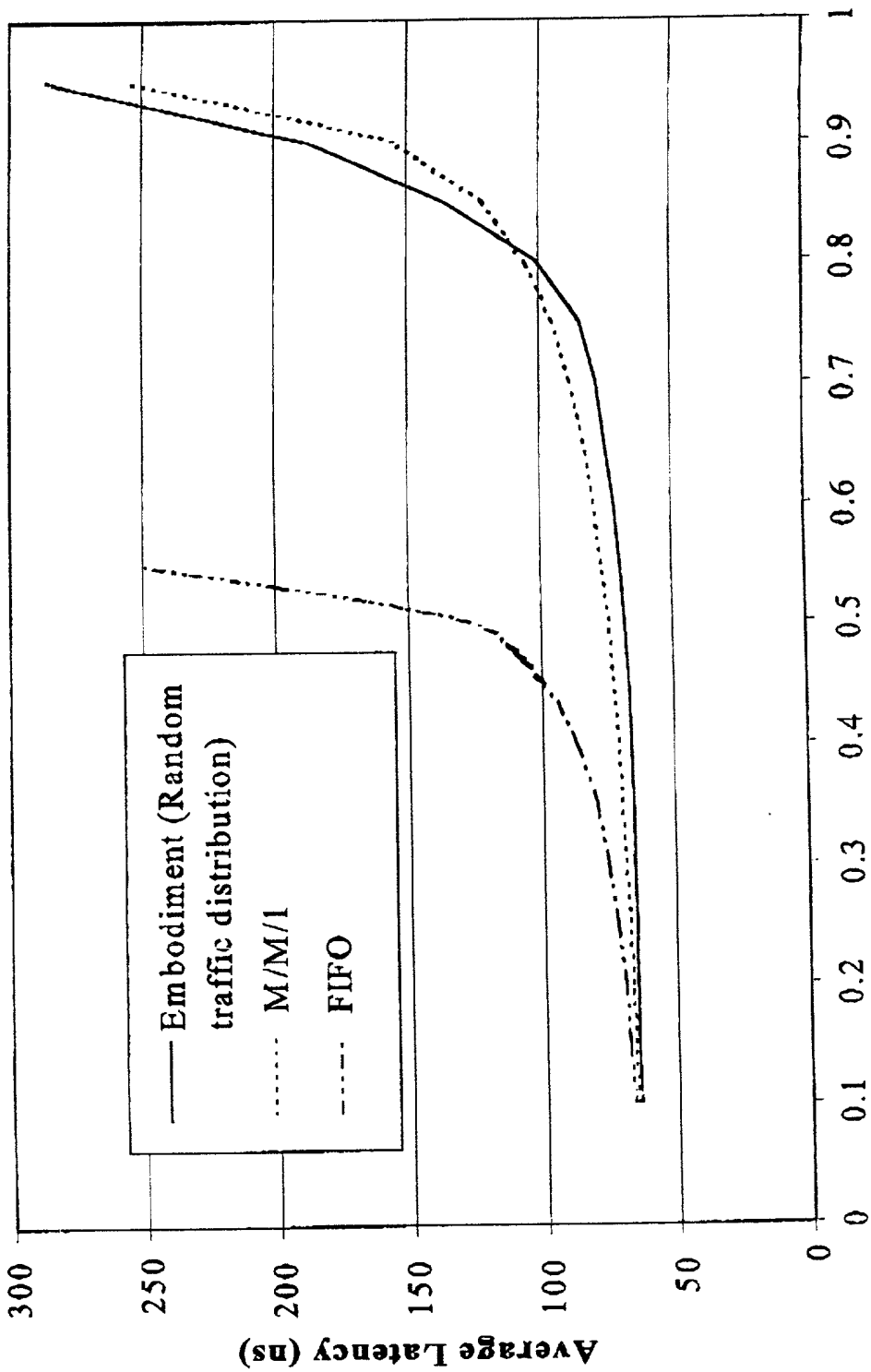

Loaded Latency
Embodiment (Random traffic distribution)
M/M/1
FIFO
Average Latency (ns)
300
250
200
150
100
50
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Load

*Fig. 7*

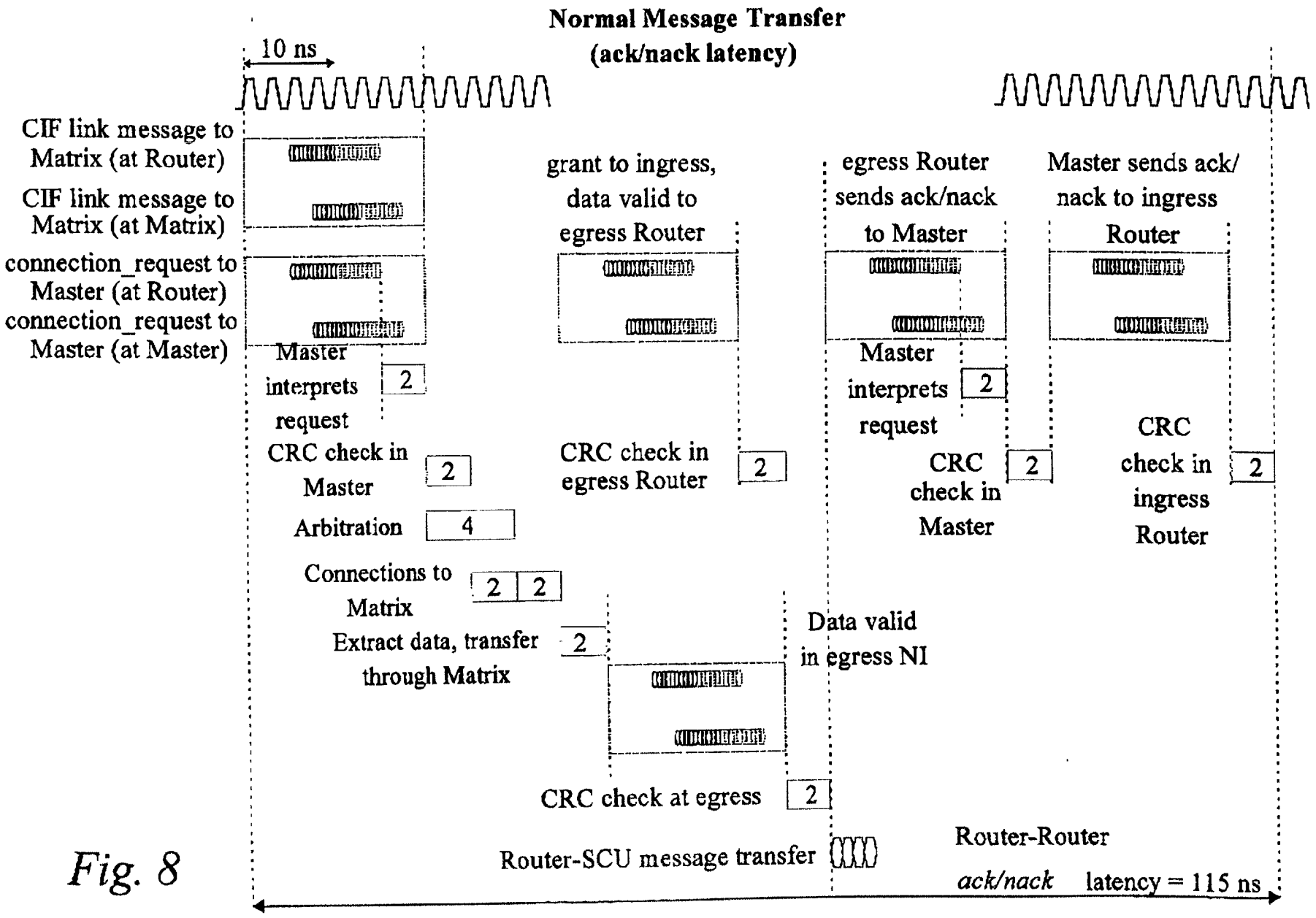

Normal Message Transfer
(ack/nack latency)
10 ns
CIF link message to Matrix (at Router)
CIF link message to Matrix (at Matrix)
connection_request to Master (at Router)
connection_request to Master (at Master)
Master interprets request
2
CRC check in Master
2
Arbitration
4
Connections to Matrix
2
2
Extract data, transfer through Matrix
2
grant to ingress, data valid to egress Router
CRC check in egress Router
2
Data valid in egress NI
CRC check at egress
2
egress Router sends ack/nack to Master
Master interprets request
2
CRC check in Master
2
Master sends ack/ nack to ingress Router
CRC check in ingress Router
2
Router-SCU message transfer
Router-Router ack/nack latency = 115 ns

*Fig. 8*